AMENDMENTS TO THE CLAIMS

1. (Original) A DLL circuit having a dummy delay corresponding to delay between an internal clock delay and an external clock, a variable delay addition circuit having a means for adjusting delay amount according to a delay amount adjustment signal, and a phase comparison circuit for comparing a phase of an internal clock with a phase of a delay clock input via the variable delay addition circuit and the dummy delay and outputting the delay amount adjustment signal to the variable delay addition circuit, the DLL circuit comprising:

a means for inputting a first signal output during 1 clock cycle of the internal clock to the variable delay addition circuit through the dummy delay at a start of burst; and

a means for detecting duration time of an active logic value of the first signal input by the variable delay addition circuit through the dummy delay until the end of the 1 clock cycle of the internal clock and setting an initial value of delay amount of the variable delay addition circuit based on the duration time at the start of burst.

2. (Original) A DLL circuit having a dummy delay corresponding to delay between an internal clock delay and an external clock, a variable delay addition circuit having a means for adjusting delay amount according to a delay amount adjustment signal, and a phase comparison circuit for comparing a phase of an internal clock with a phase of a delay clock input via the variable delay addition circuit and the dummy delay and outputting the delay amount adjustment signal to the variable delay addition circuit, the DLL circuit comprising:

a means for inputting a first signal set at a logic "1" during 1 clock cycle of the internal clock to the variable delay addition circuit through the dummy delay at a start of burst; and a means for detecting duration time of the logic "1" of the first signal input by the variable delay addition circuit through the dummy delay until the end of the 1 clock cycle of the internal clock and setting an initial value of delay amount of the variable delay addition circuit based on the duration time at the start of burst.

3. (Original) A DLL circuit having a dummy delay corresponding to delay between an internal clock delay and an external clock, a variable delay addition circuit having a means for adjusting delay amount according to a delay amount adjustment signal, and a phase comparison circuit for comparing a phase of an internal clock with a phase of a delay clock input via the variable delay addition circuit and the dummy delay and outputting the delay amount adjustment signal to the variable delay addition circuit, the DLL circuit comprising:

a means for inputting a first signal set at a logic "1" during 1 clock cycle of the internal clock to the variable delay addition circuit through the dummy delay as an initialization mode at a start of burst;

a means for detecting duration time of the logic "1" of the first signal input by the variable delay addition circuit through the dummy delay until the end of the 1 clock cycle of the internal clock and setting an initial value of delay amount of the variable delay addition circuit based on the duration time as the initialization mode at the start of burst; and

a clock output means for generating an output clock that synchronizes with the external clock one clock cycle behind with the internal clock delayed by the variable delay addition circuit and with the delay amount corrected by the phase comparison circuit as a lock mode after the initial setting of the delay amount in the variable delay addition circuit.

4. (Currently Amended) The DLL circuit according to any one of claims 1 to 3, wherein the internal clock and the output clock are completely stopped when a reading operation is not performed~~, thereby achieving a standby mode and a clock can be output in an extremely short time from start of the reading operation~~.

5. (Original) The DLL circuit according to any one of claims 1 to 3 further comprising a means for setting a delay value of the dummy delay circuit based on a signal input from a storage means prepared in the same semiconductor chip.

6. (Currently Amended) The DLL circuit according to any one of claims 1 to 3, wherein a delay element in the variable delay addition circuit is formed of an inverter circuit and a circuit having an opposite delay time characteristic to the inverter with respect to power supply voltage.

7. (Original) The DLL circuit according to any one of claims 1 to 3, wherein it is possible to prevent hazard from occurring in a DLL output clock by synchronizing switching timing of delay amount adjustment of the variable delay addition circuit with the output clock of the variable delay addition circuit instead of the internal clock.

8. (Original) A delay element comprising an inverter and a transfer gate, wherein variations in delay time due to variations in power supply voltage can be minimized by supplying electric potential having dependency opposite to increase and decrease in power source voltage to a gate input of the transfer gate.

9. (Currently Amended) The DLL circuit according to claim 1, wherein the [[A]] variable delay addition circuit comprises ~~comprising~~ a delay element having an inverter and a clocked inverter and a register as a counterpart of the delay element, wherein the register automatically stores a logic value of a delay signal at the time when the clocked inverter becomes disabled.

10. (Original) A phase comparison circuit comprising a multistage inverter and a clocked inverter and comparing a phase of a reference signal with a phase of a delay signal by latching the delay signal at the time when the clocked inverter is disabled by a reference clock.